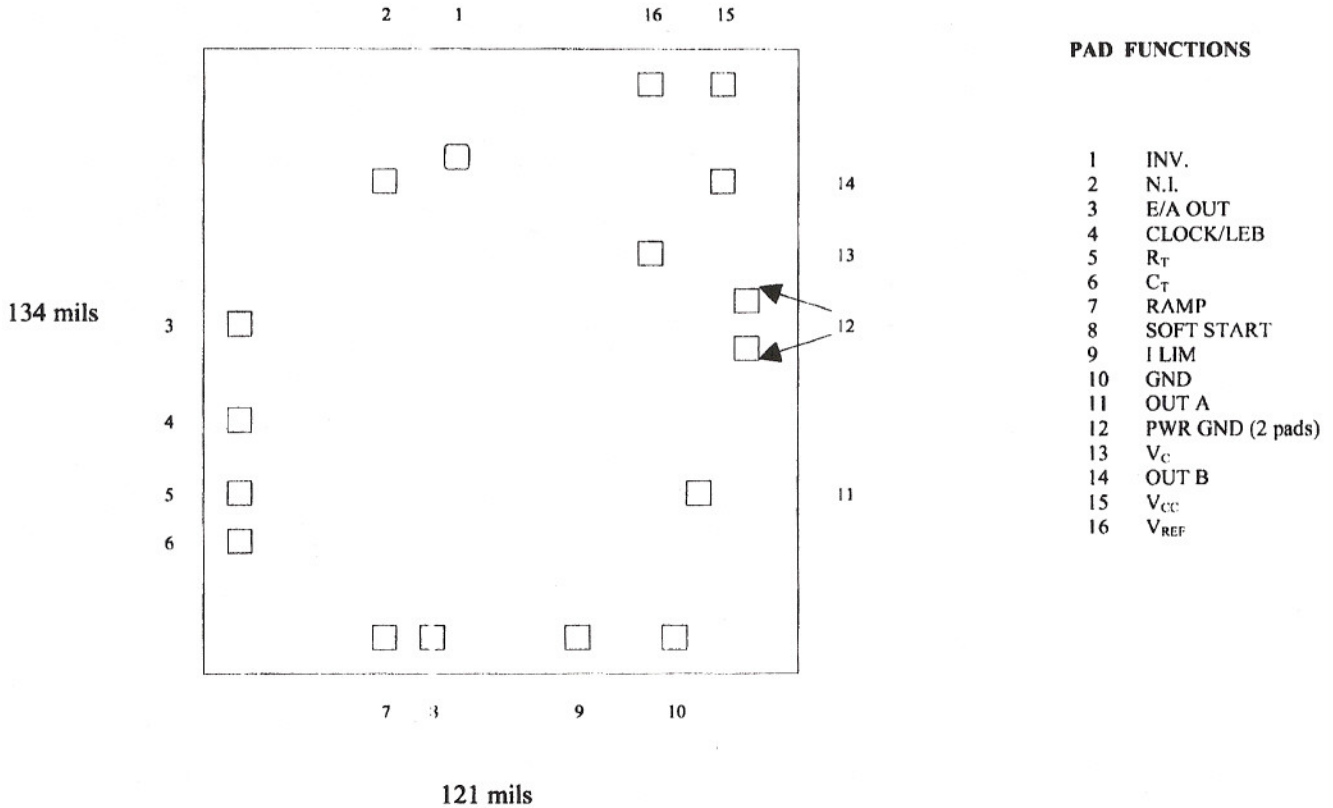




Sierra Components, Inc.

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PAD FUNCTIONS

- 1 INV.
- 2 N.I.
- 3 E/A OUT
- 4 CLOCK/LEB
- 5 R_T
- 6 C_T
- 7 RAMP
- 8 SOFT START
- 9 I LIM
- 10 GND
- 11 OUT A
- 12 PWR GND (2 pads)
- 13 V_c
- 14 OUT B
- 15 V_{cc}
- 16 V_{REF}

NOTE: Both PWR GND pads must be connected

The information given is believed to be correct at the time of issue.
 Please verify your requirements prior to commencement of any assembly process, as no liability for omission or error can be accepted.
 Chip back potential is the level at which bulk silicon is maintained either by bond pad connection or in some cases the potential to which the chip back must be connected if stated above.

Note: 1 mil = 0.001inch

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| <p><u>APPROVED</u></p> <p>G.Bibby</p> <p>.....</p> <p>DATE: 23 Oct 2003</p> | <p>UC2823B</p> <p>UNITRODE</p> | <p><u>DIE INFORMATION</u></p> <p>DIMENSIONS (Mils): 121 x 134 x 15</p> <p>BOND PADS (Mils): 4 x 4 min</p> <p>MASK. REF: JJ</p> <p>GEOMETRY:</p> <p>BACK POTENTIAL: GND</p> |
| <p>DG 10.1.2</p> <p>Rev B, 7/19/02</p> | | <p><u>METALLISATION</u></p> <p>TOP: Al</p> <p>BACK: Si</p> |